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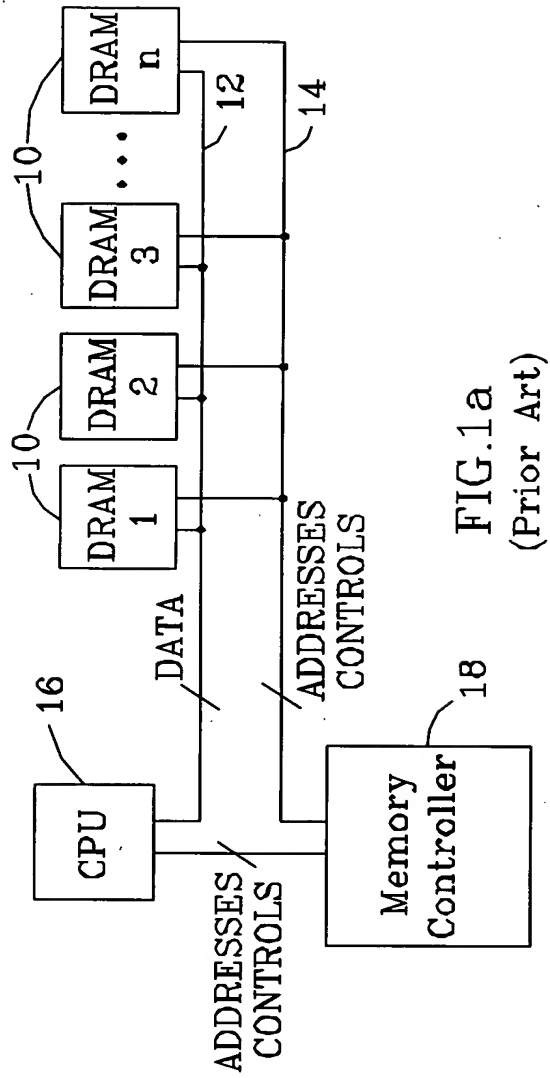


FIG. 1a
(Prior Art)

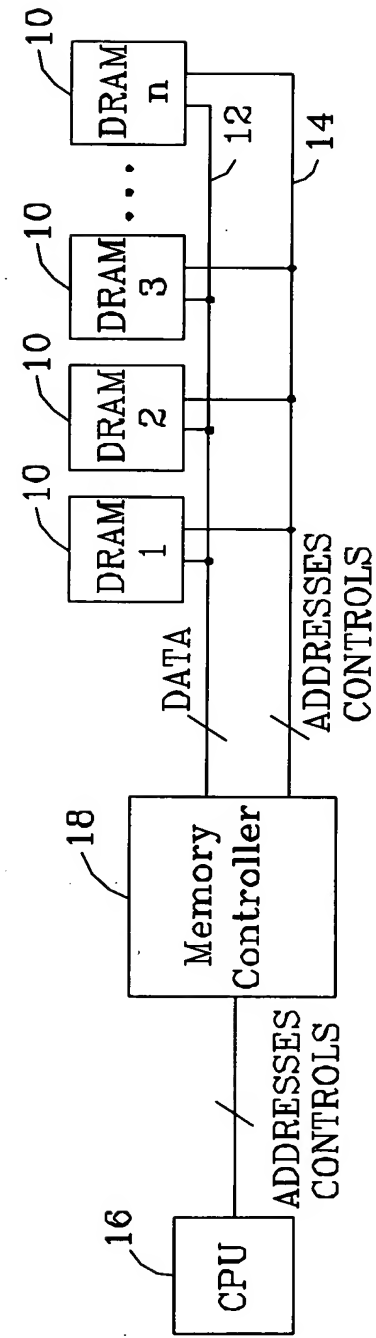


FIG. 1b
(Prior Art)

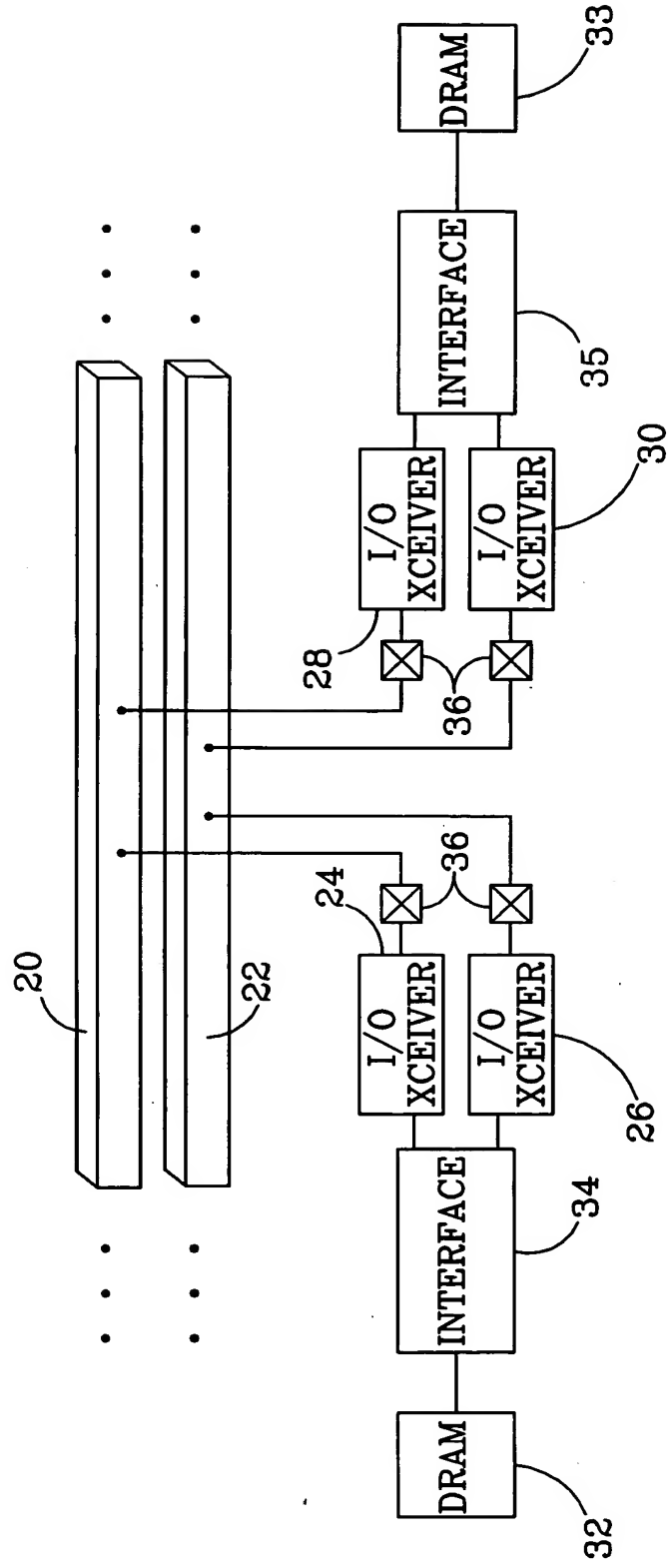
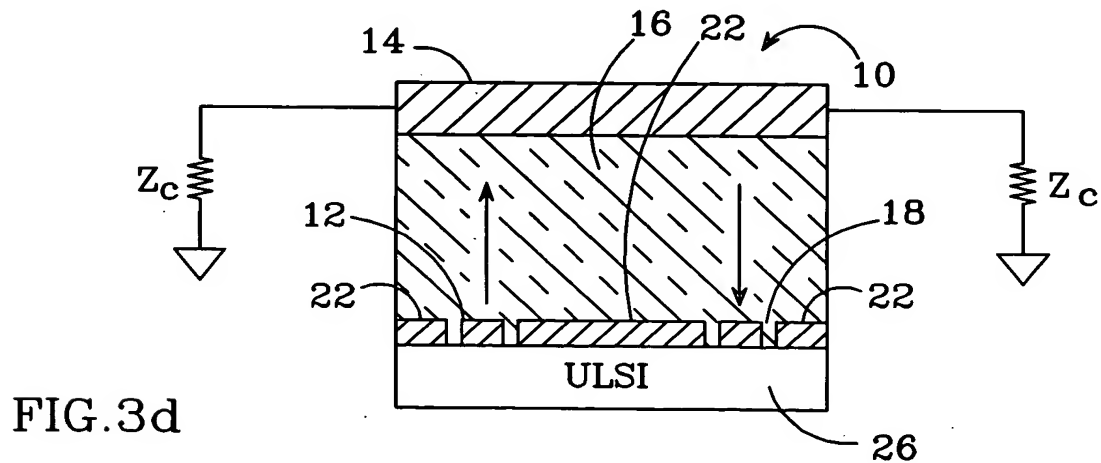
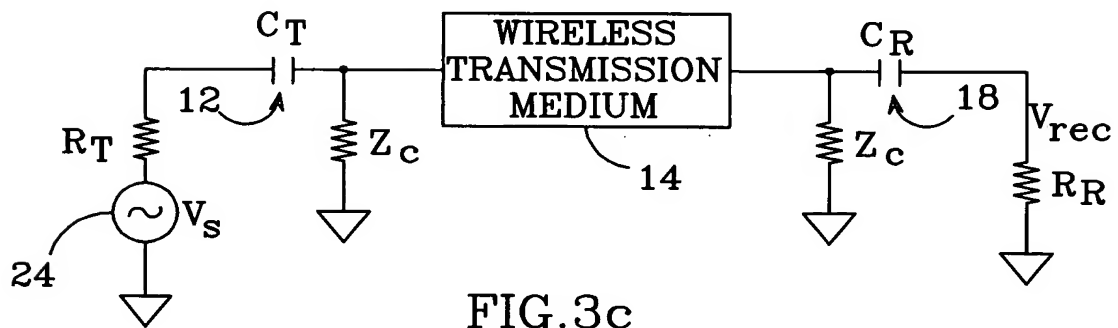
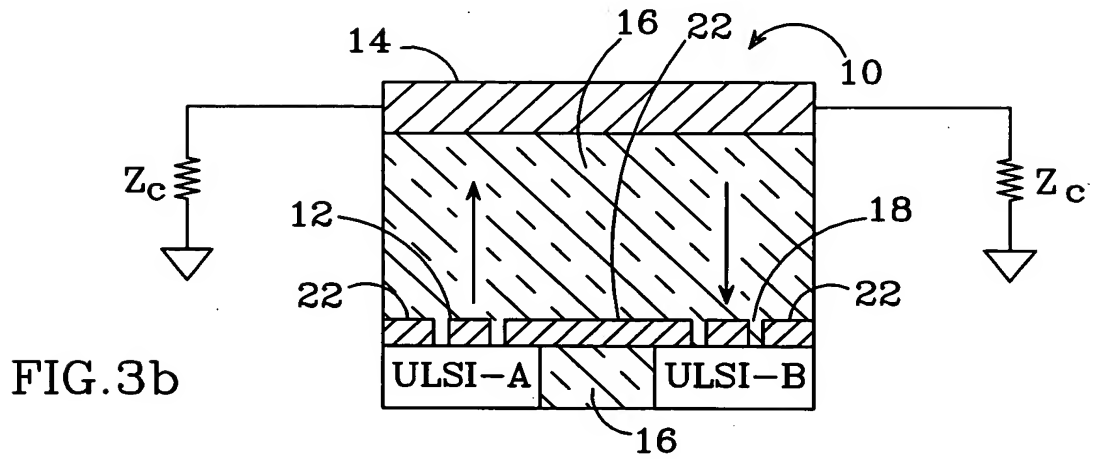
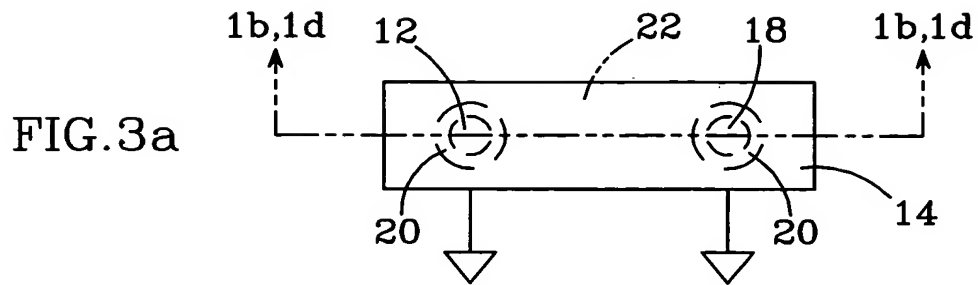
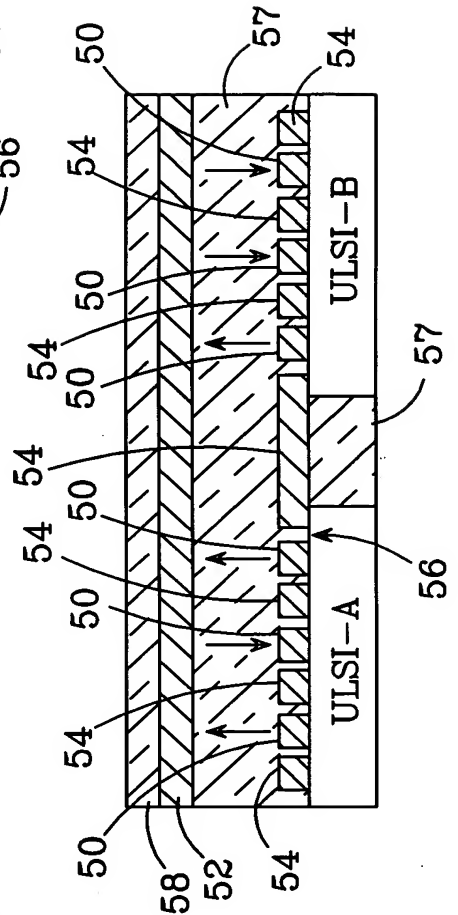
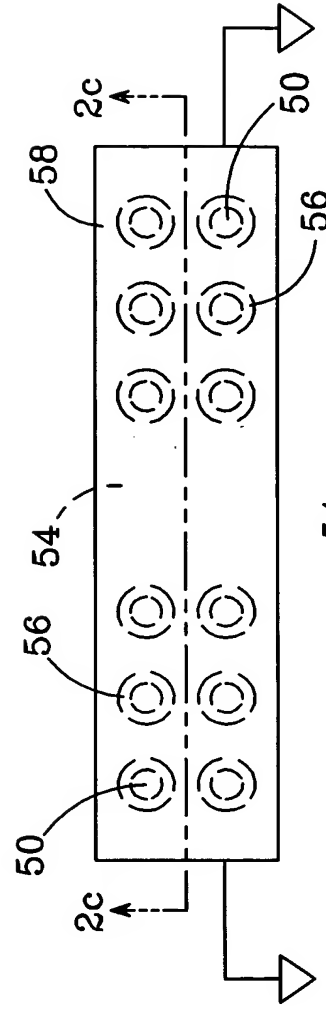
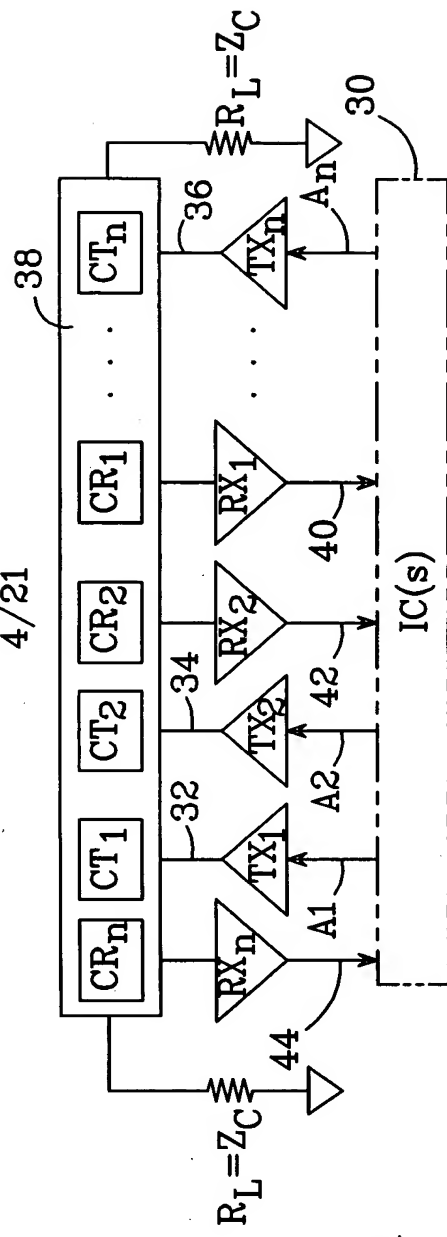


FIG. 2
(Prior Art)





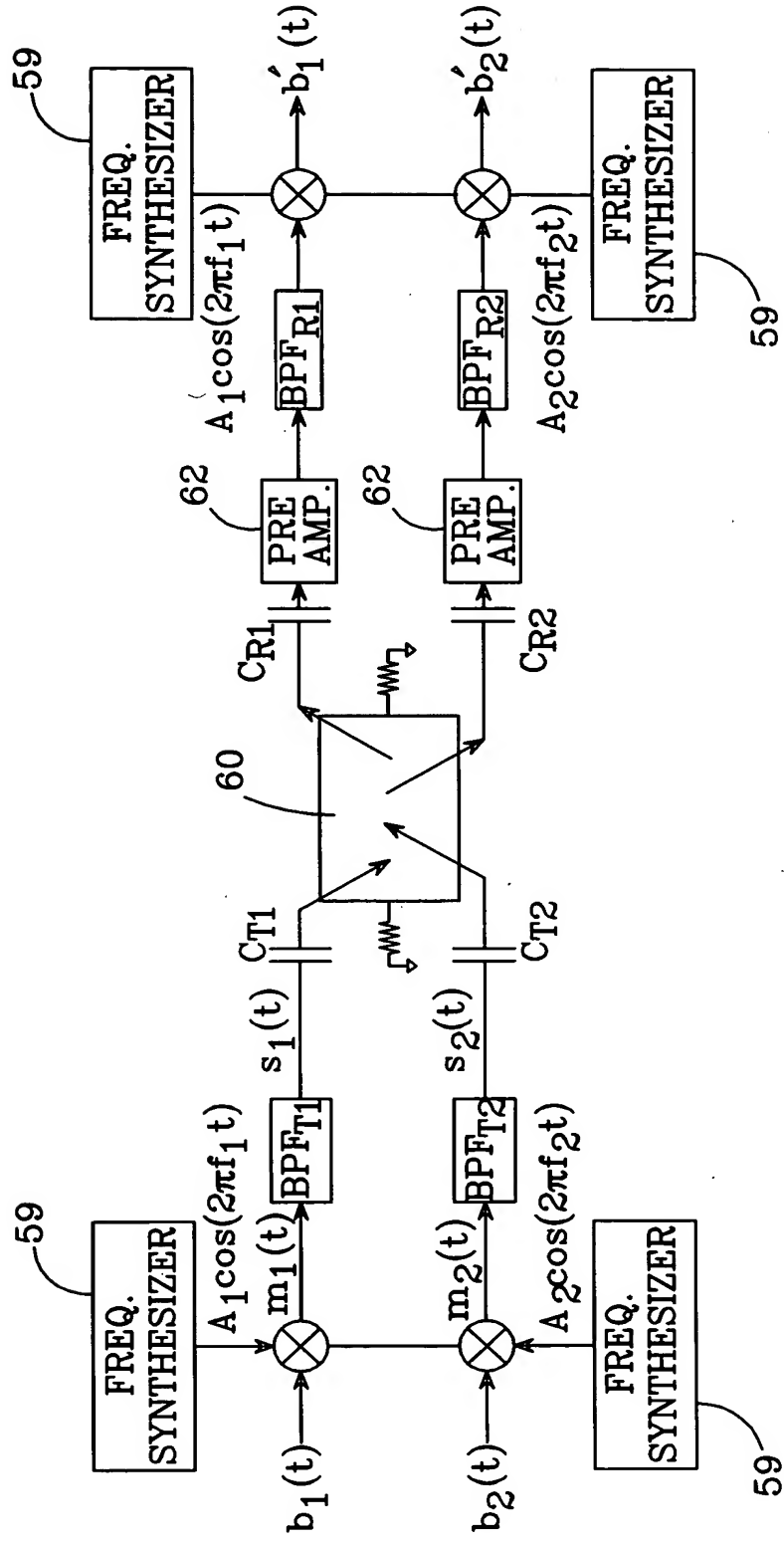


FIG. 5

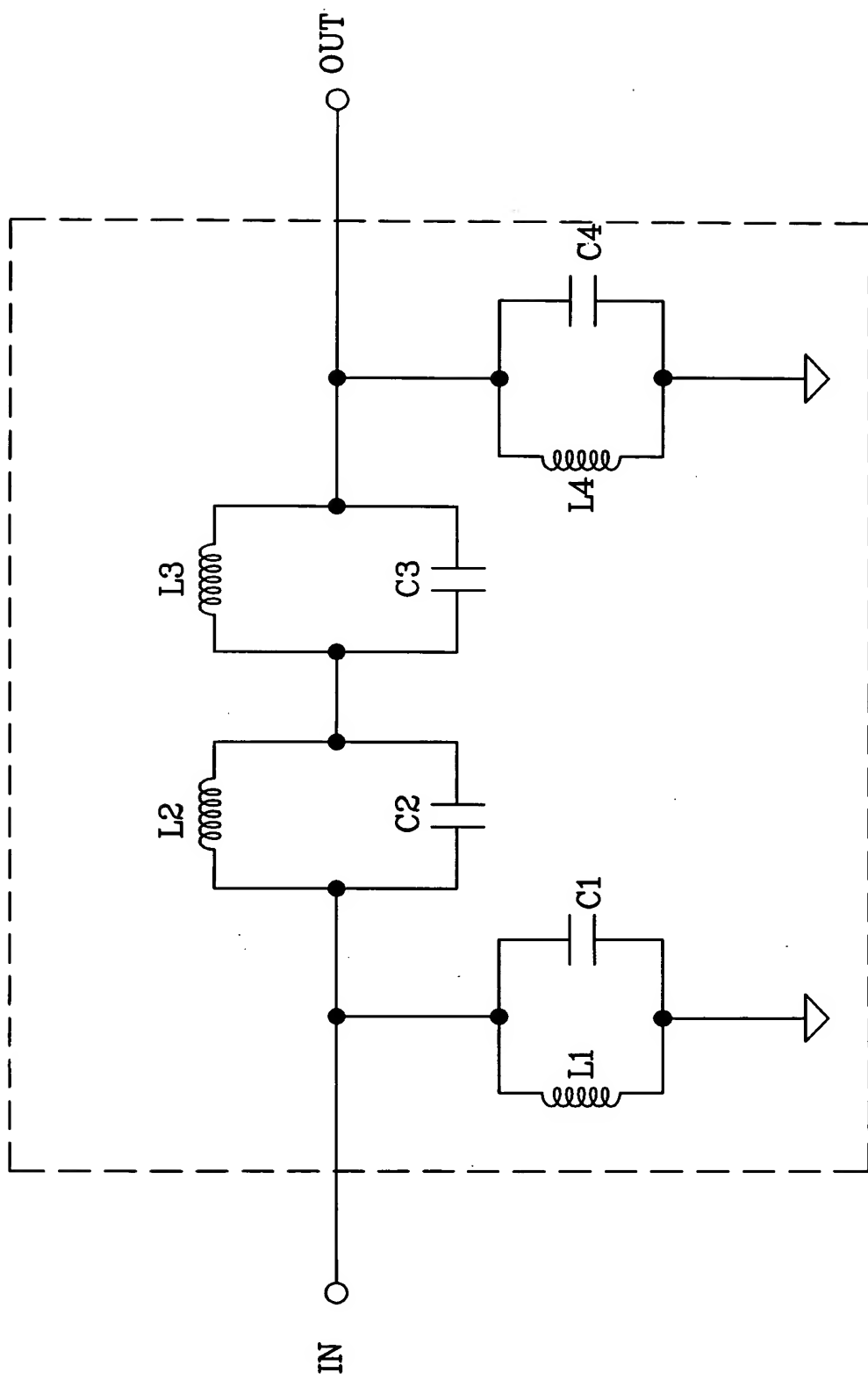


FIG.6

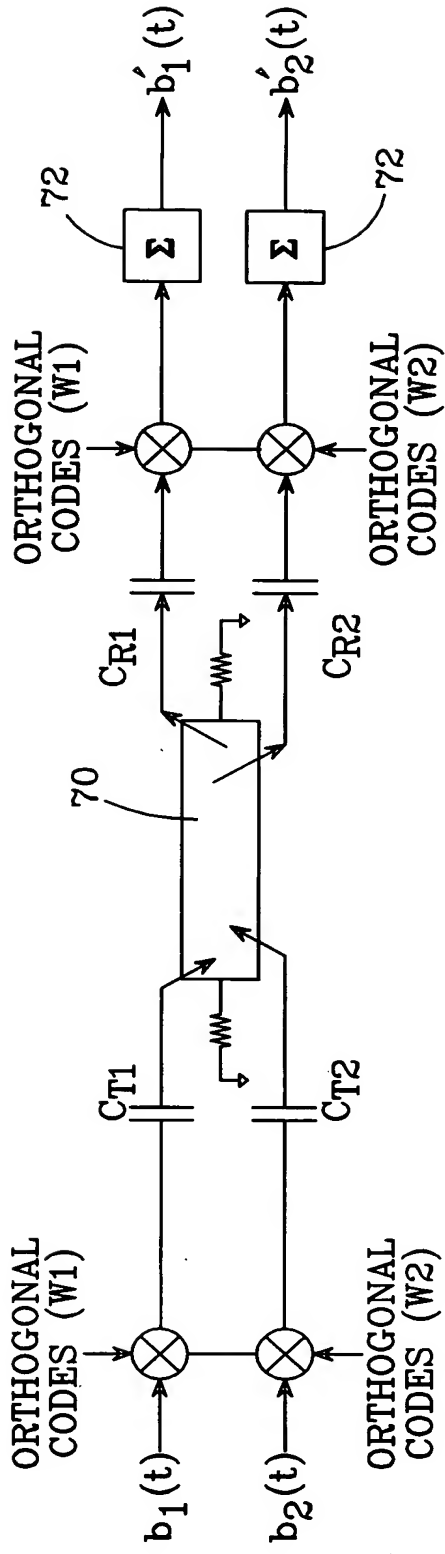


FIG. 7

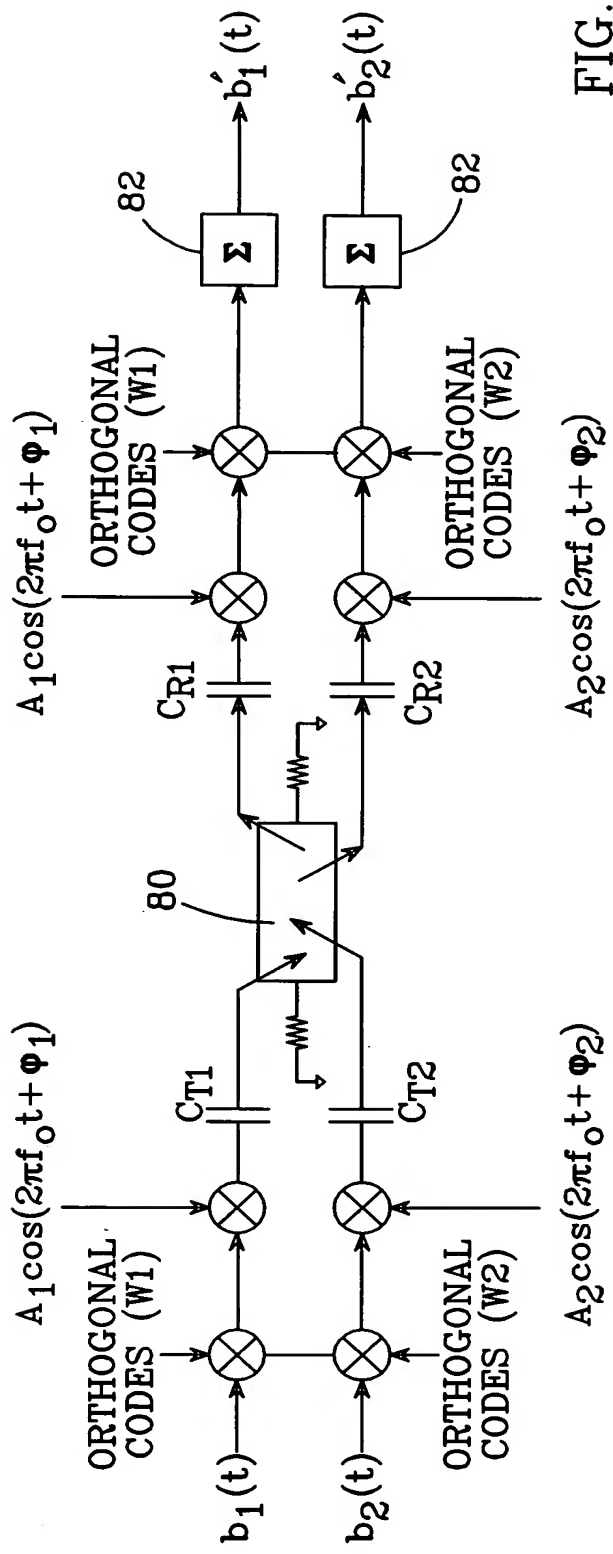


FIG. 8

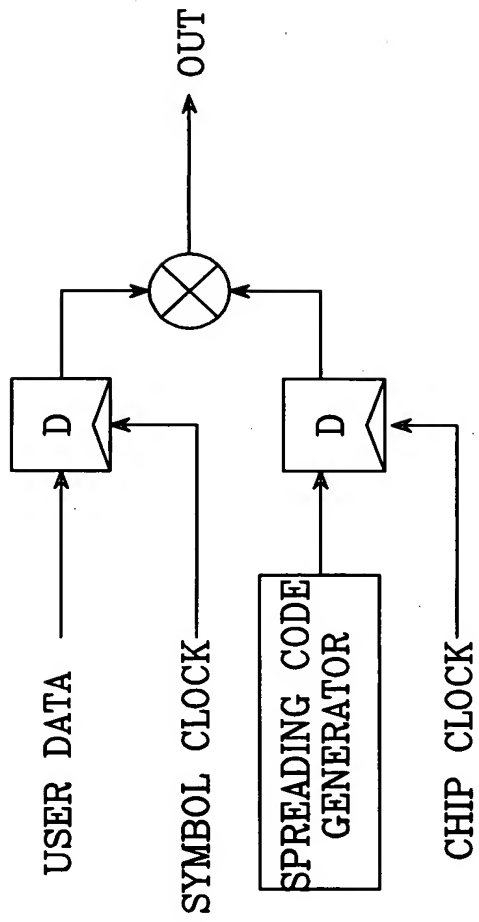


FIG. 9a

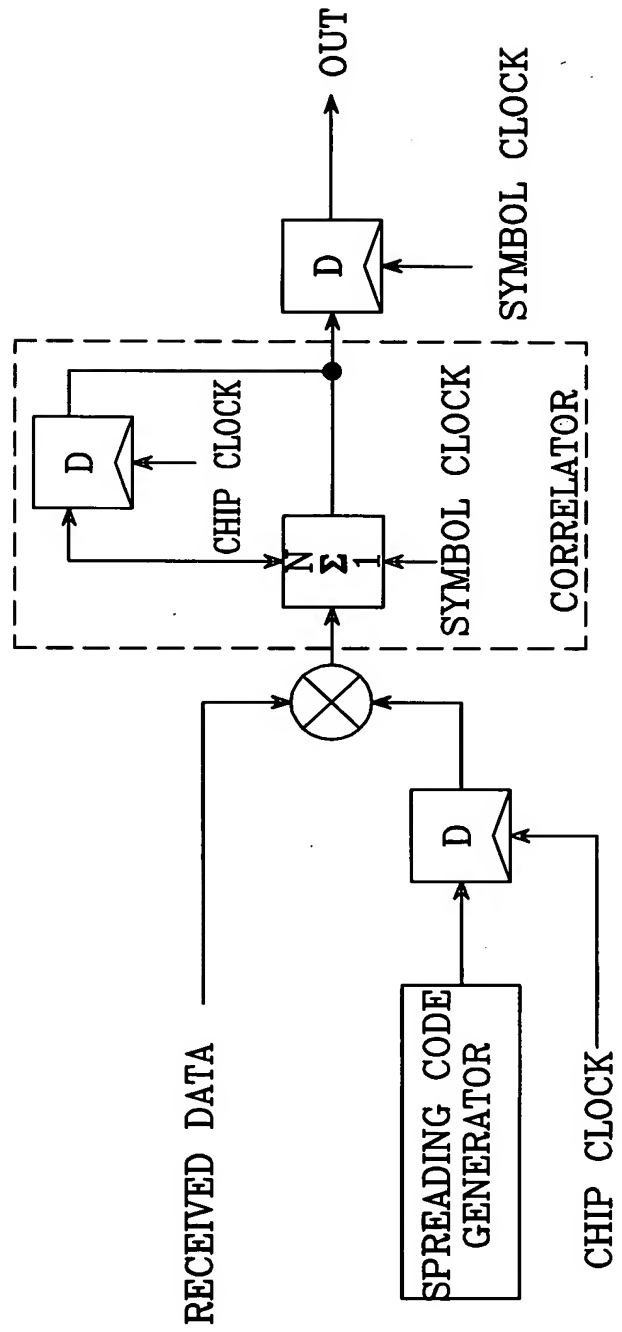


FIG. 9b

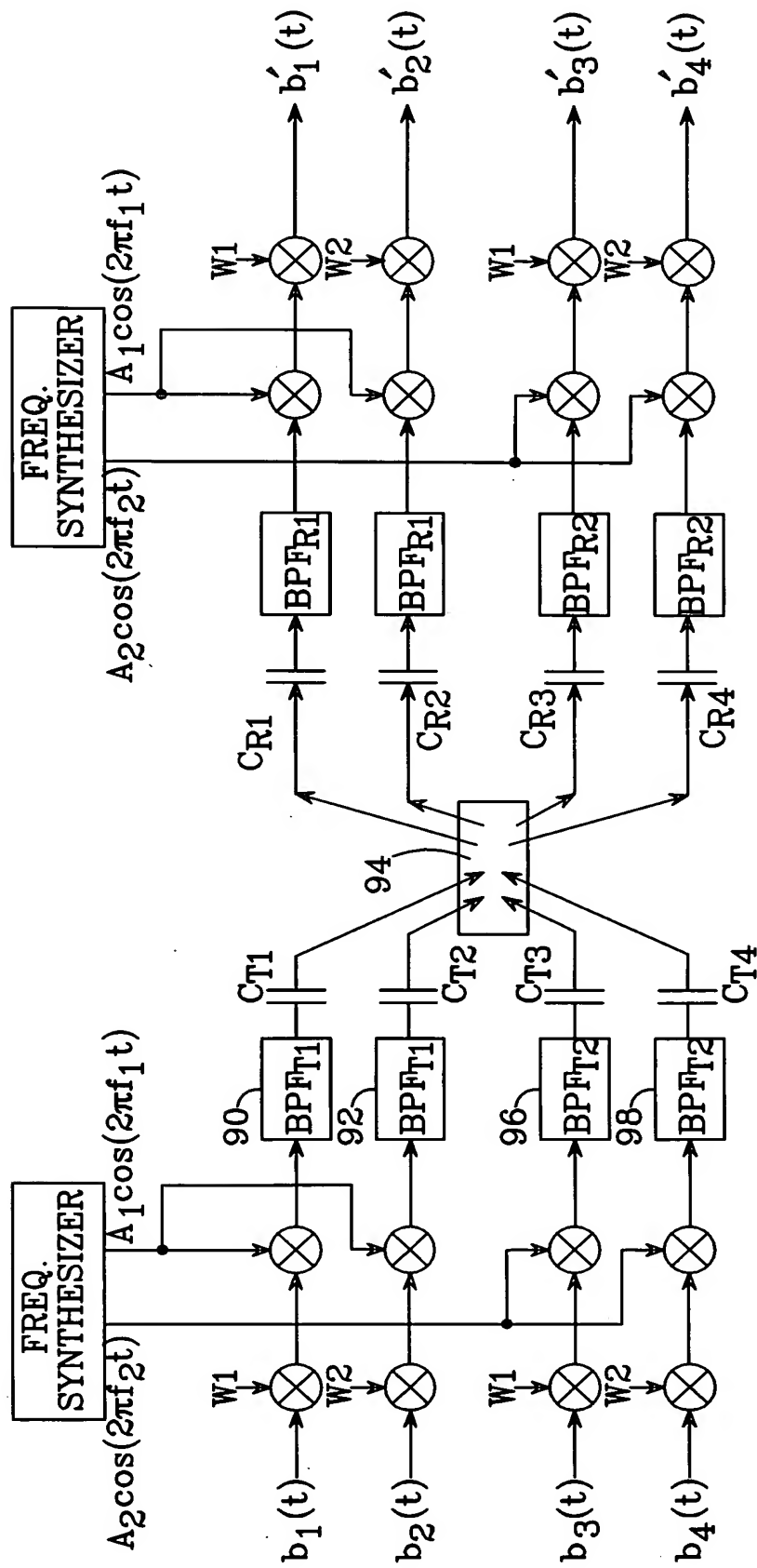


FIG.10

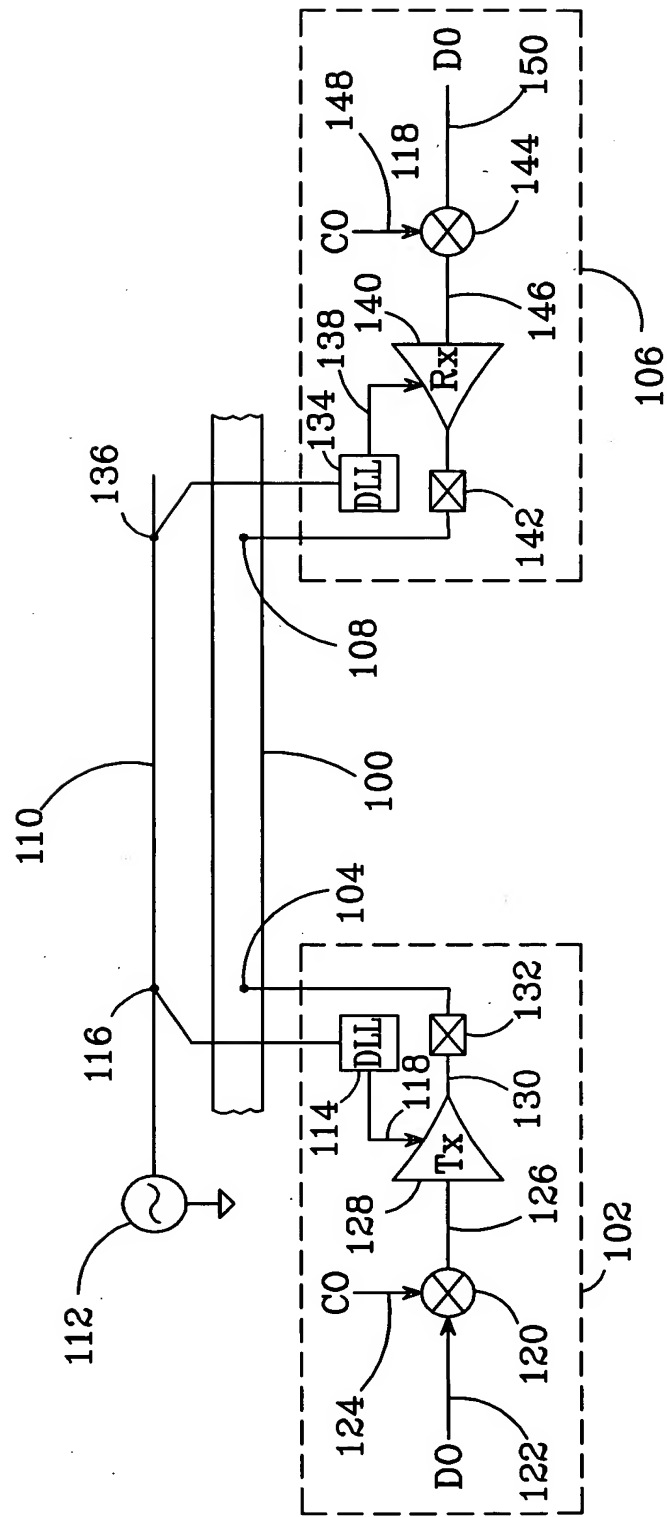


FIG.11

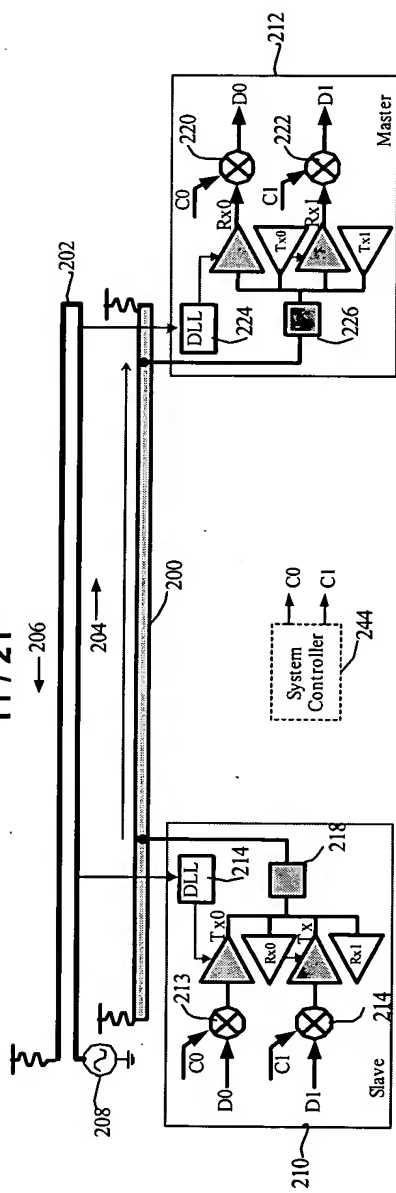


Fig. 12 a

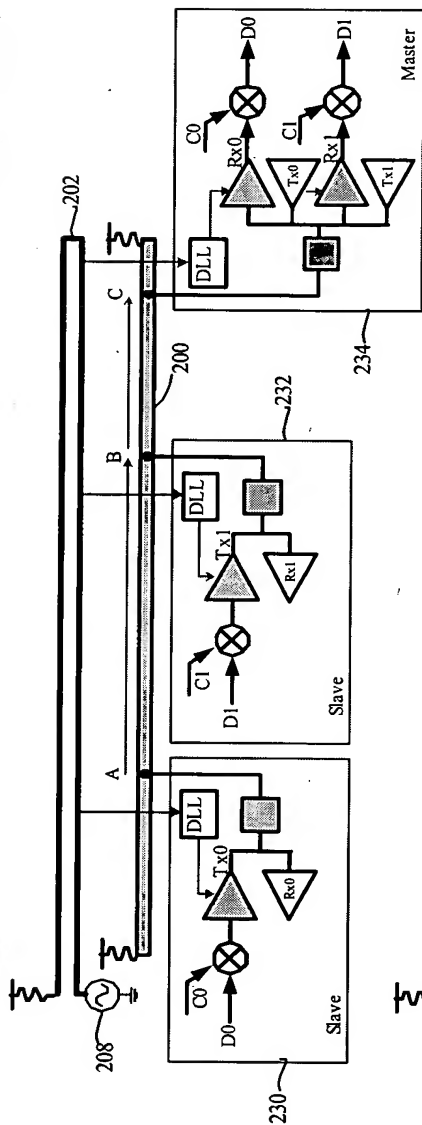


Fig. 12 b

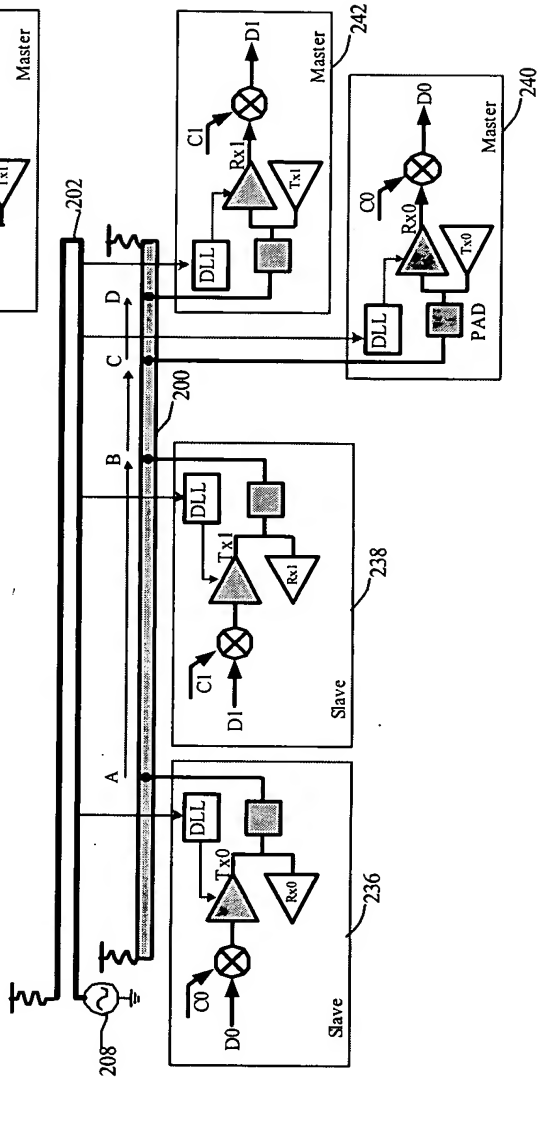


Fig. 12 c

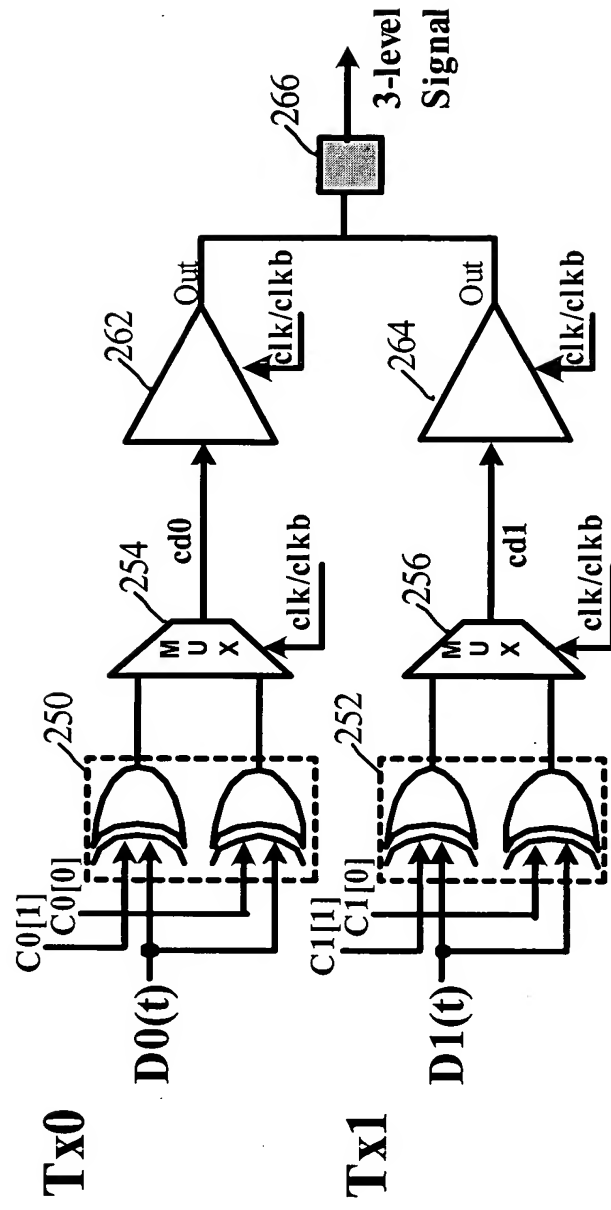


FIG. 13

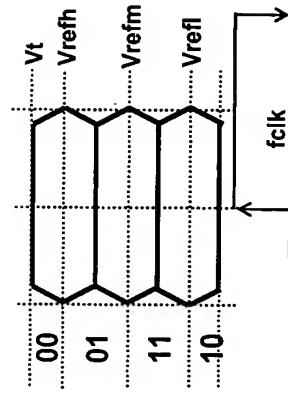


Fig. 14 a

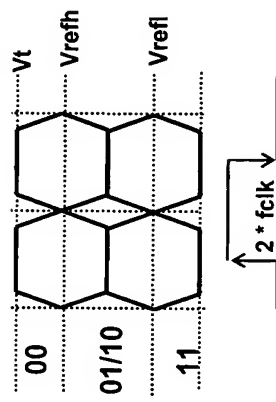


Fig. 14 b

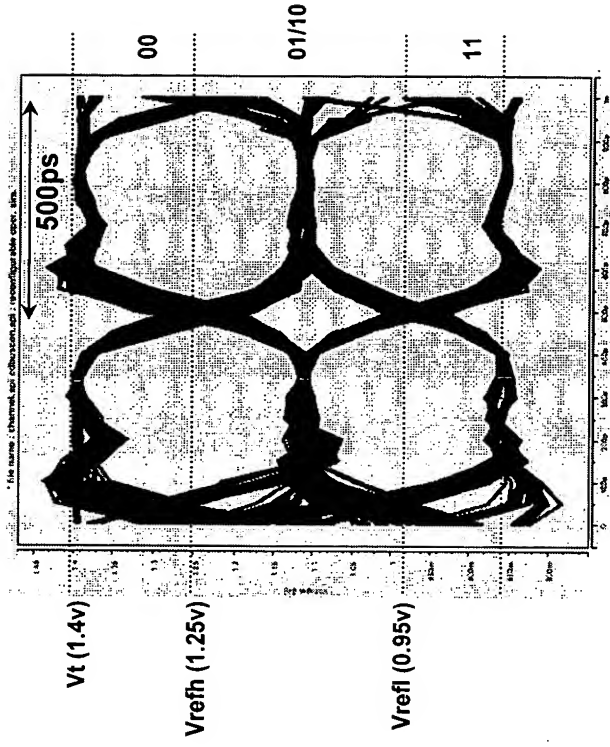


Fig. 14 c

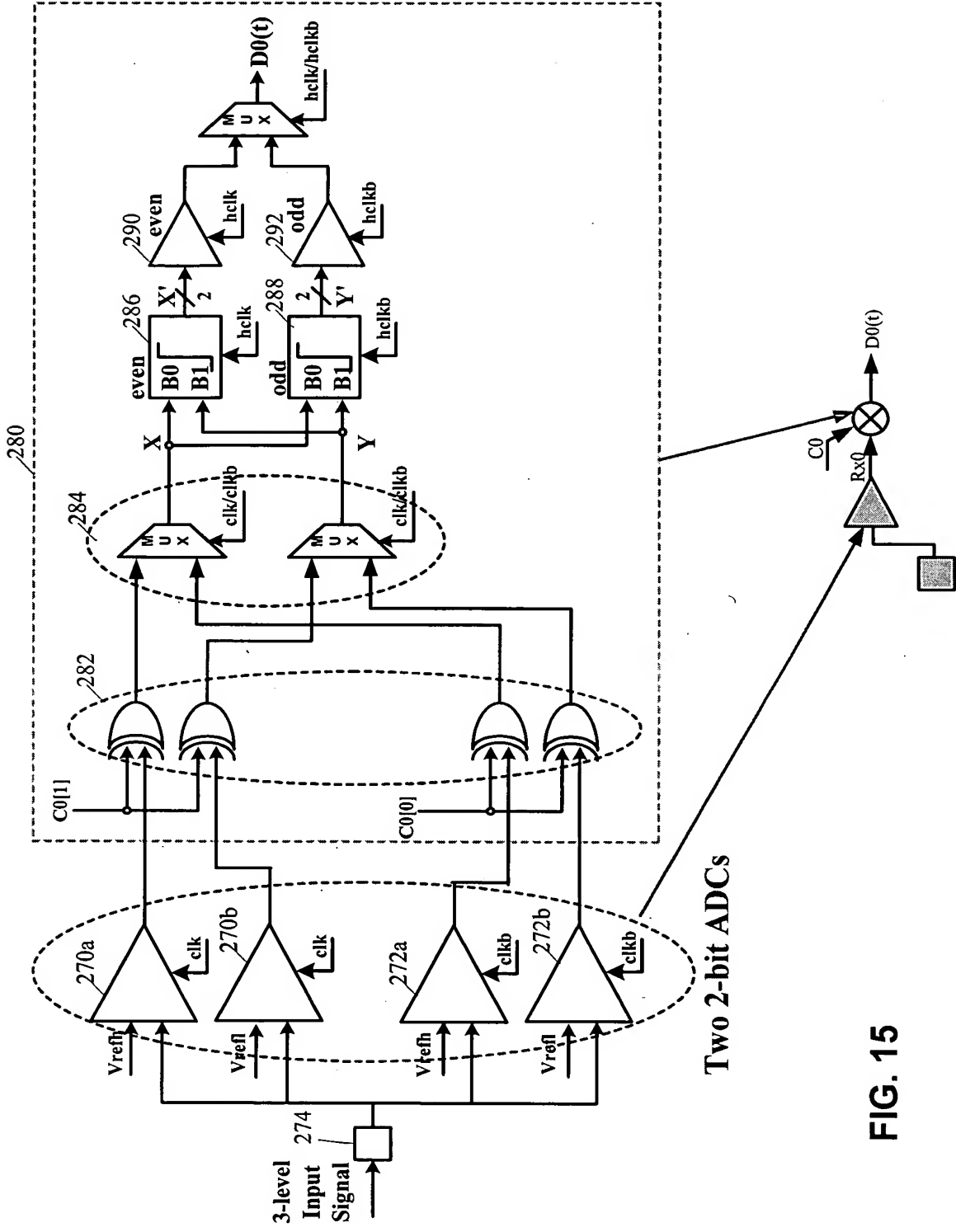


FIG. 15

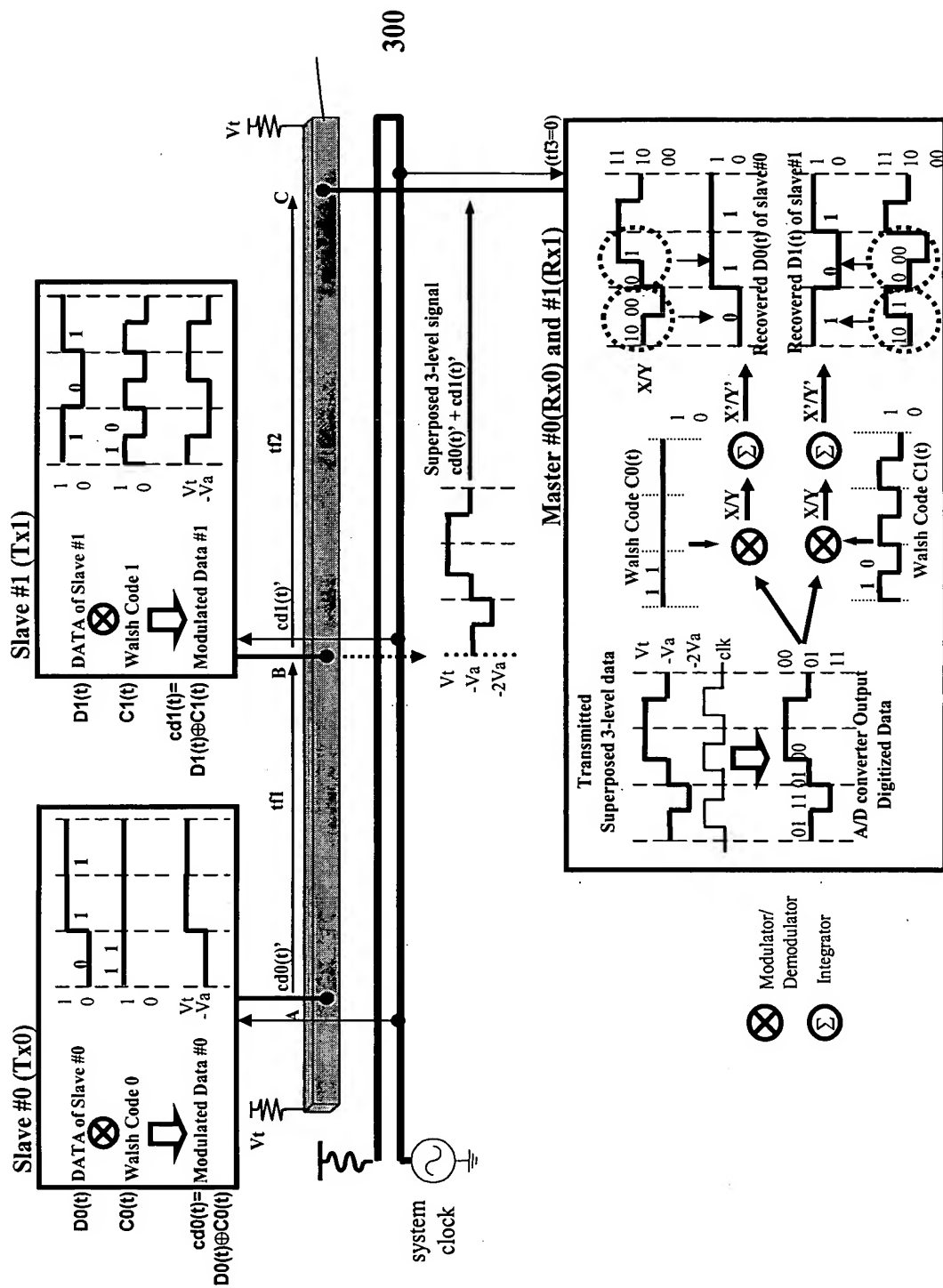


FIG. 17

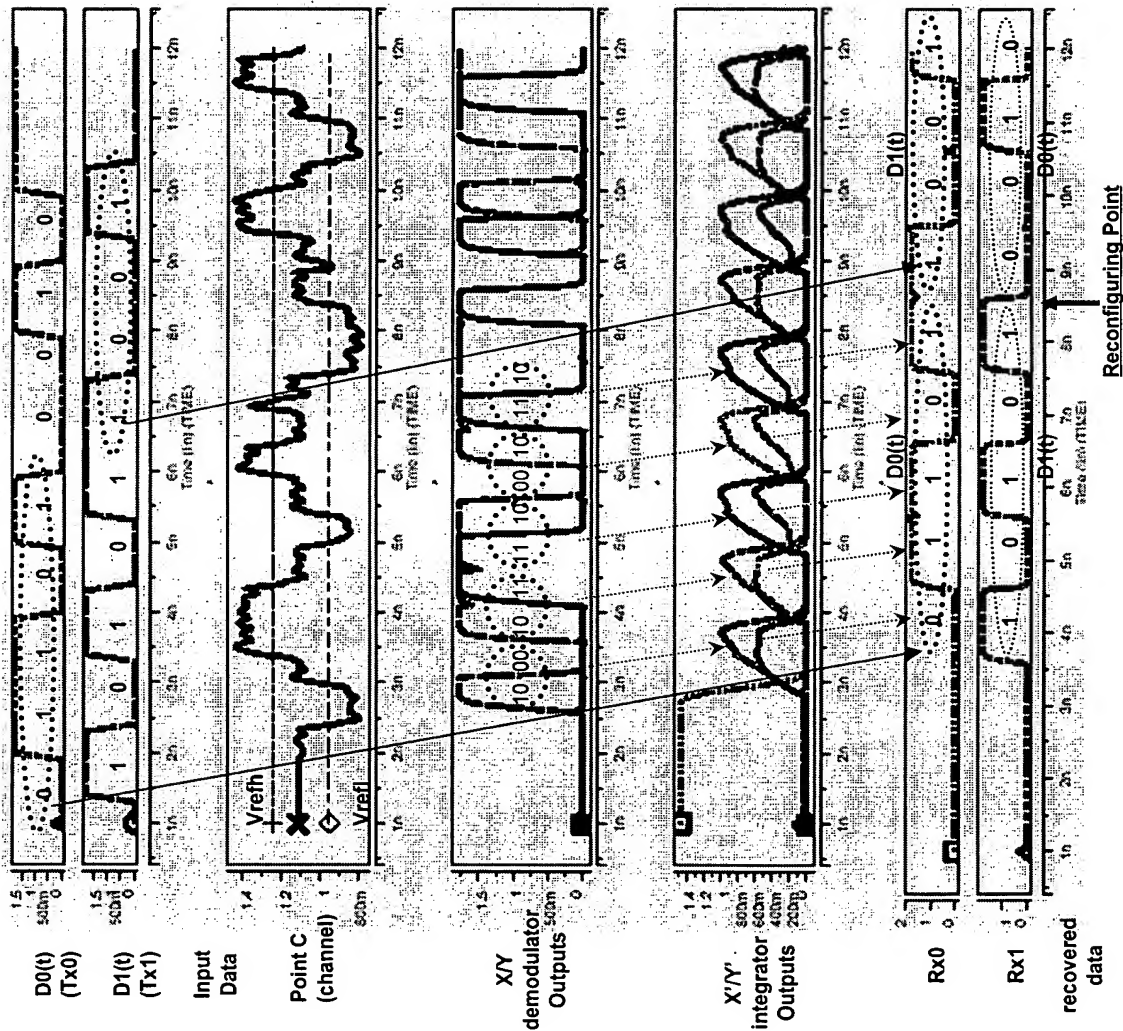
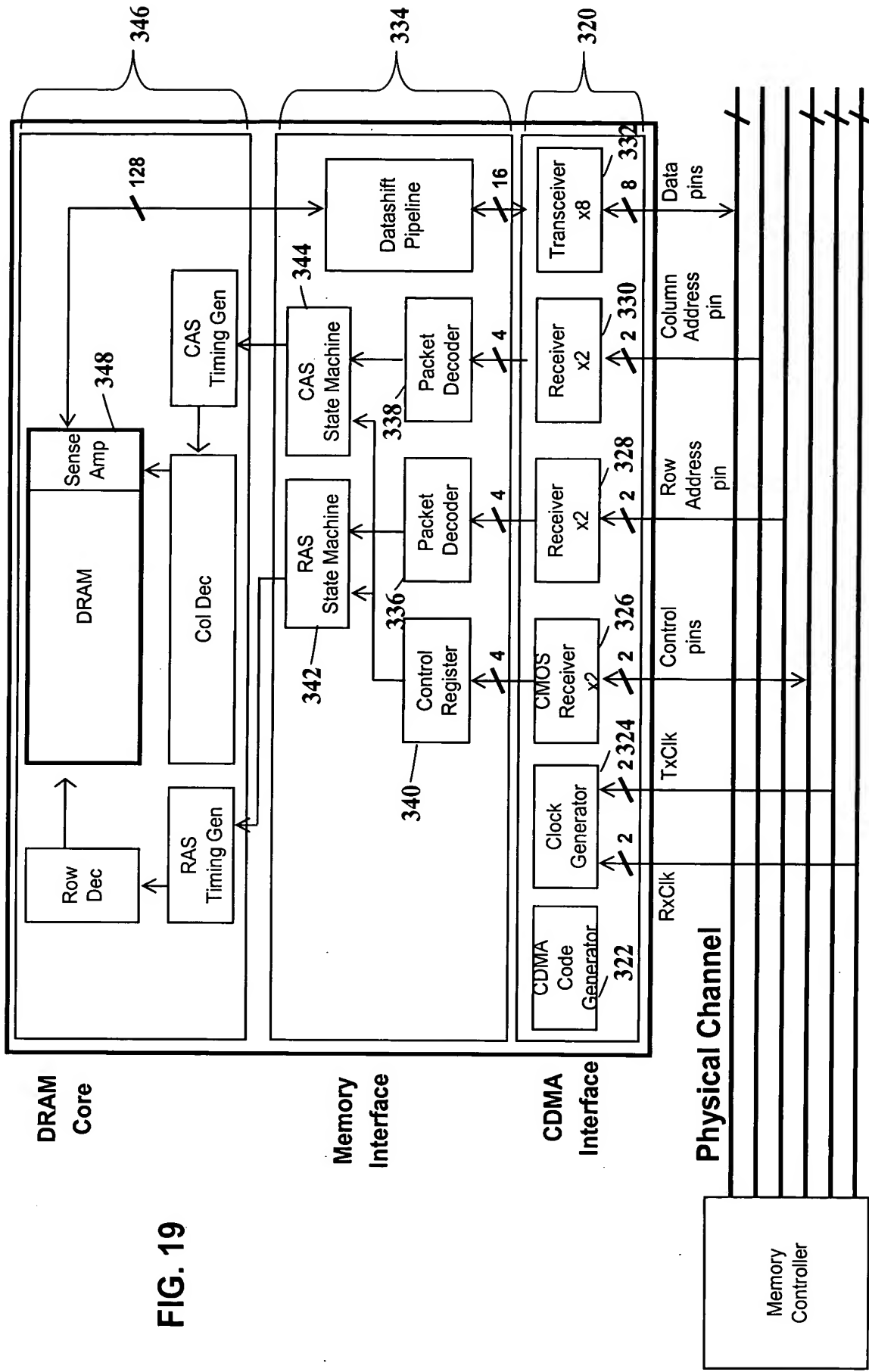


FIG. 18

FIG. 19



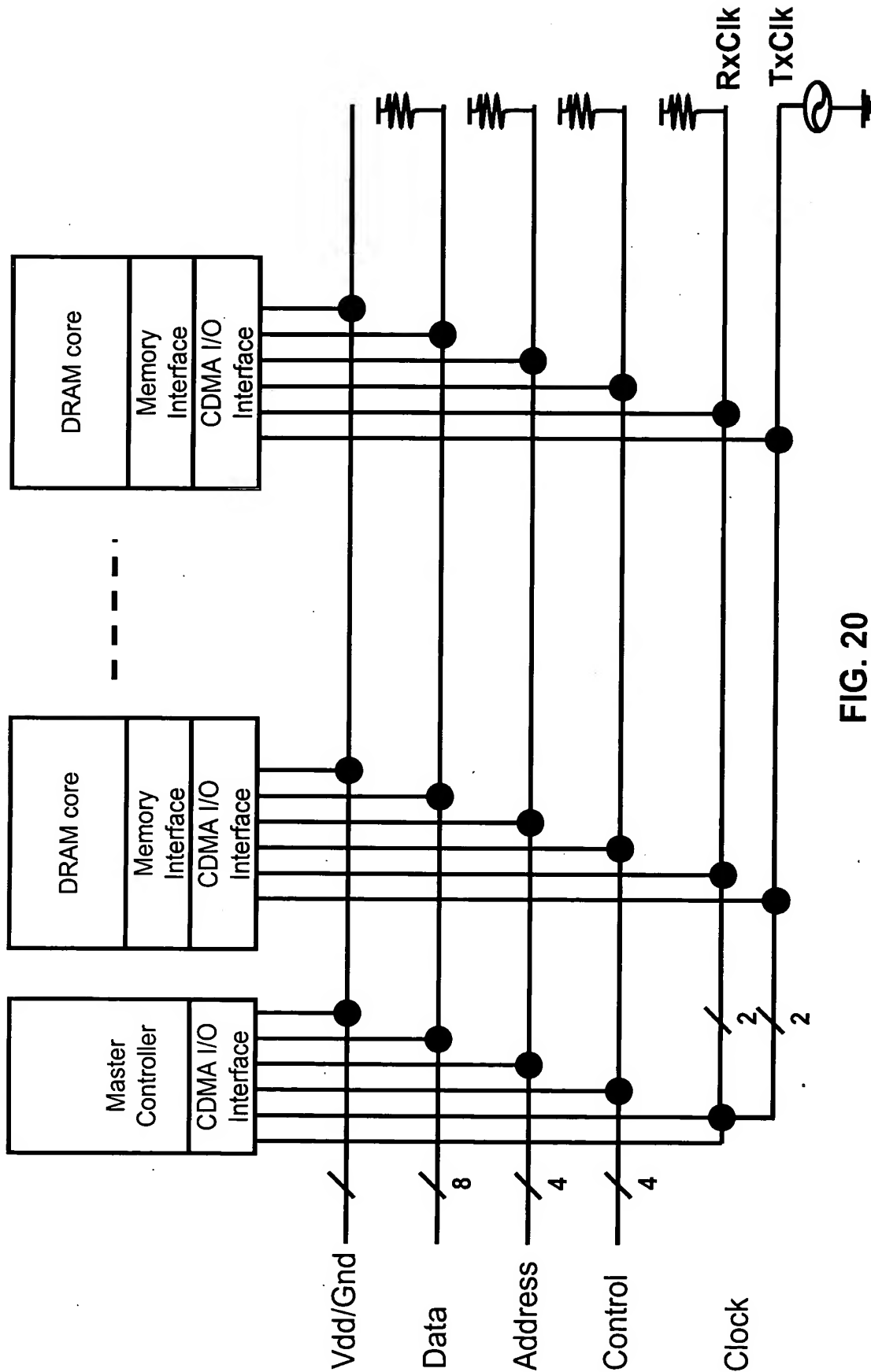
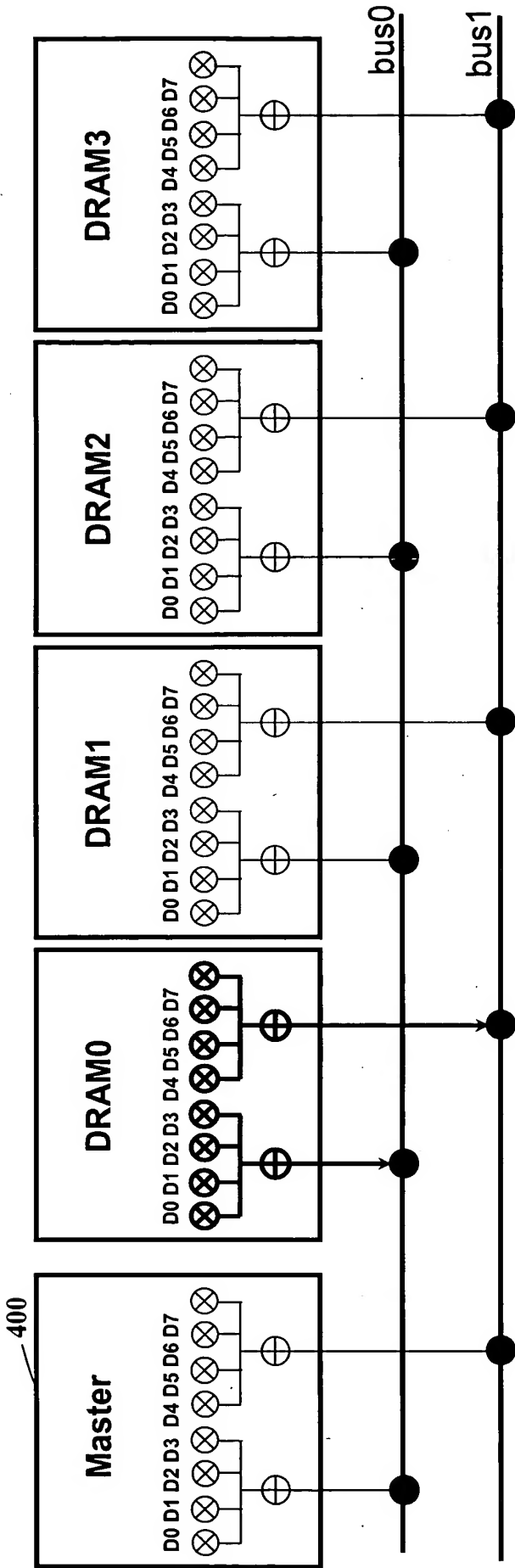
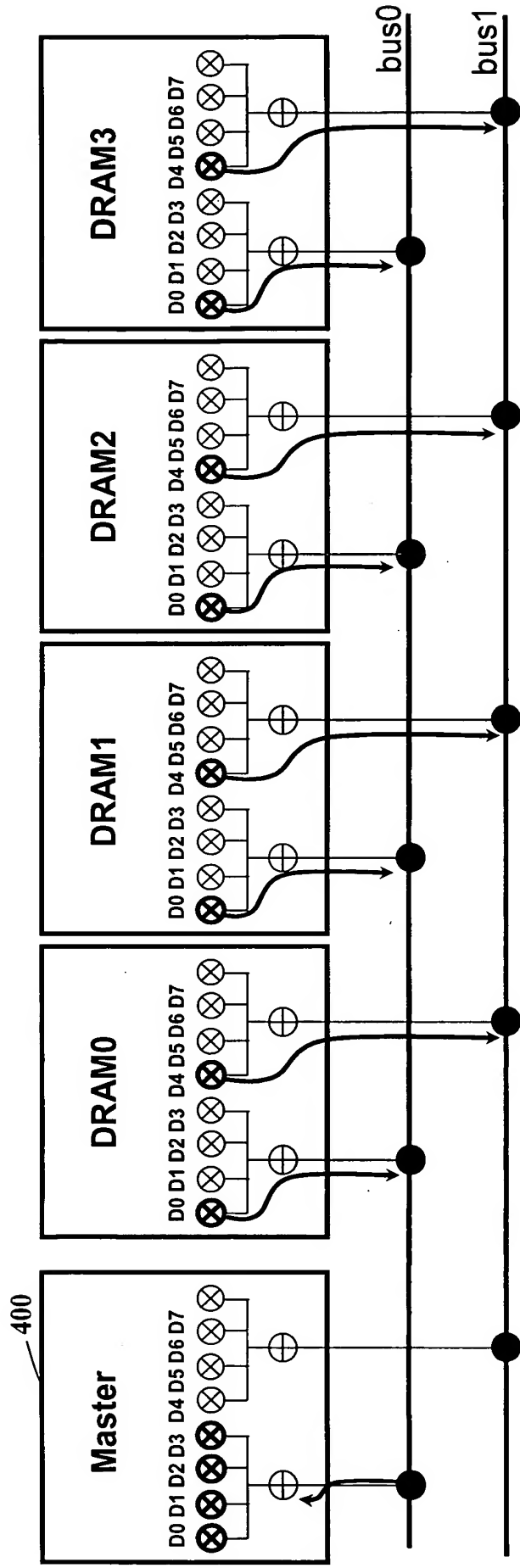


FIG. 20



DQ	CDMA Code							
	Master	DRAM0	DRAM1	DRAM2	DRAM3			
D0	W0	W0	-	-	-			
D1	W1	W1	-	-	-			
D2	W2	W2	-	-	-			
D3	W3	W3	-	-	-			
D4	W4	W4	-	-	-			
D5	W5	W5	-	-	-			
D6	W6	W6	-	-	-			
D7	W7	W7	-	-	-			

FIG. 21



DQ	CDMA Code							
	Master	DRAM0	DRAM1	DRAM2	DRAM3			
D0	W0	W0	W1	W2	W3			
D1	W1	-	-	-	-			
D2	W2	-	-	-	-			
D3	W3	-	-	-	-			
D4	W4	W4	W5	W6	W7			
D5	W5	-	-	-	-			
D6	W6	-	-	-	-			
D7	W7	-	-	-	-			

FIG. 22